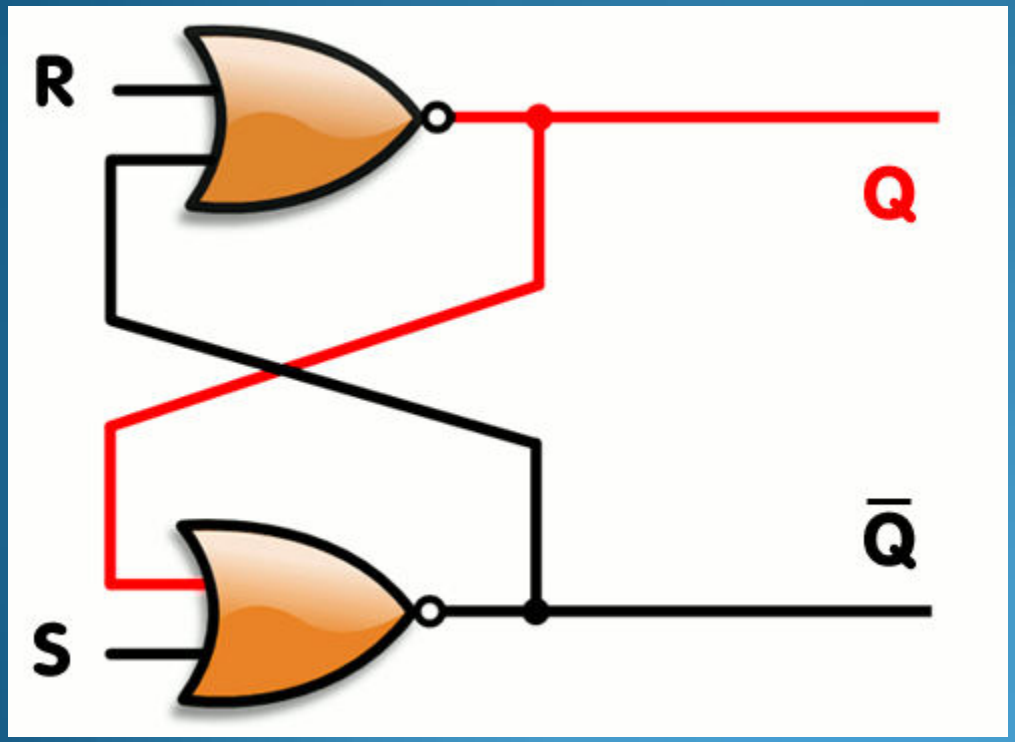
Date:10 October 2018

Today's Topics

- SR latch : using NOR and NAND gates
- SR Flip Flop: using NOR and NAND gates
- D Flip Flop: Eliminating the draw backs of SR FF

Flip Flops



- It is a bistable Multivibrator made up of NOR or NAND gates.
- It is used as a memory element to store a bit.
- Non-Clocked FF is also called a latch. Figure shows RS latch

A Truth table and working of RS FF

R	S	Q	Action
0	0	Last value	No change
0	1	1	Set
1	0	0	Reset
1	1	?	Forbidden

FIG. 8-4 Truth table for a NOR–gate *RS* flip-flop

defined as R and S. The input/output possibilities for this *RS* flip-flop are summarized in the truth table in Fig. 8–4. To aid your understanding of the operation of this circuit, recall that a logic 1 at any input of a NOR gate forces its output to a logic 0.

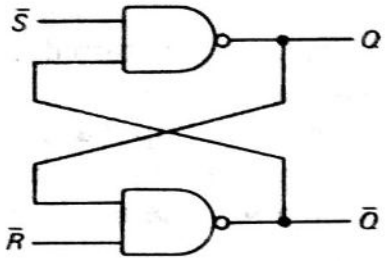
The first input condition in the truth table is $R = 0$ and $S = 0$. Since a 0 at the input of a NOR gate has no effect on its output, the flip-flop simply remains in its present state; that is, Q remains unchanged.

The second input condition $R = 0$ and $S = 1$ forces the output of NOR gate B low. Both inputs to NOR gate A are now low, and the NOR-gate output must be high. Thus a 1 at the S input is said to *SET* the flip-flop, and it switches to the stable state where $Q = 1$.

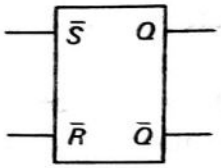
The third input condition is $R = 1$ and $S = 0$. This condition forces the output of NOR gate A low, and since both inputs to NOR gate B are now low, the output must be high. Thus a 1 at the R input is said to *RESET* the flip-flop, and it switches to the stable state where $Q = 0$ (or $\overline{Q} = 1$).

The last input condition in the table, $R = 1$ and $S = 1$, is forbidden, as it forces the outputs of both NOR gates to the low state. In other words, both $Q = 0$ and $\overline{Q} = 0$ at the same time! But this violates the basic definition of a flip-flop that requires Q to be the complement of $\overline{Q}$, and so it is generally agreed never to impose this input condition. Incidentally, if this condition is for some reason imposed, the resulting state of Q is not predictable. That's why the truth table entry is a ?.

NAND gate latch and SR FF using NAND gates and their Truth Tables



(a) NAND gate latch

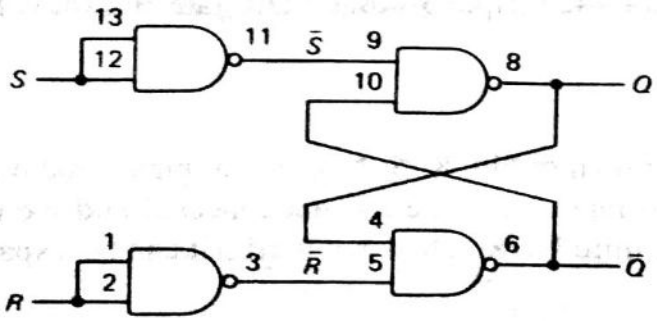


(b) Logic symbol

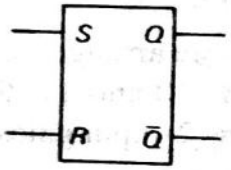
$\bar{R}$	$\bar{S}$	Q
1	1	Last state
1	0	1
0	1	0
0	0	? (Forbidden)

(c) Truth table

FIG. 8–7 $\bar{R}\bar{S}$ flip-flop



(a) 54/7400



(b) Symbol

R	S	Q
0	0	Last state
0	1	1
1	0	0
1	1	? (Forbidden)

(c)

FIG. 8–8 An *RS* flip-flop (latch)

Clocked RS FF using NAND and NOR realizations

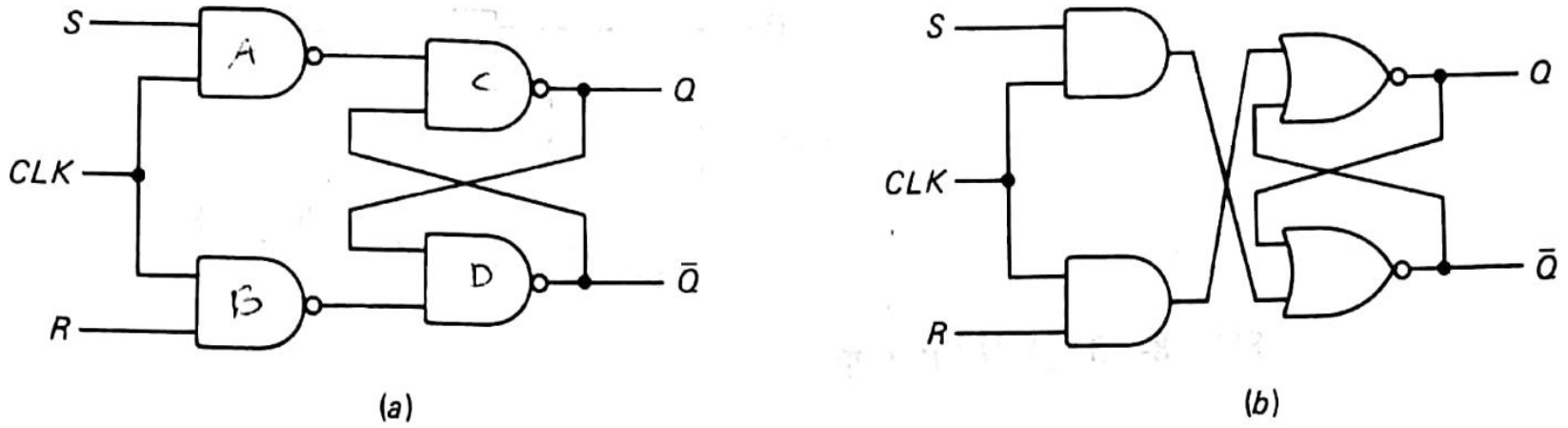


FIG. 8–11 Two different realizations for a clocked *RS* flip-flop

Use of ENABLE and Strobe

according to the truth table.

The addition of two AND gates at the R and S inputs as shown in Fig. 8–10 will result in a flip-flop that can be enabled or disabled. When the ENABLE input is low, the AND gate outputs must both be low and changes in neither R nor S will have any effect on the flip-flop output Q. The latch is said to be *disabled*.

When the ENABLE input is high, information at the R and S inputs will be transmitted directly to the outputs. The latch is said to be *enabled*. The output will change in response to input changes as long as the ENABLE is high. When the ENABLE input goes low, the output will retain the information that was present on the input when the high-to-low transition takes place.

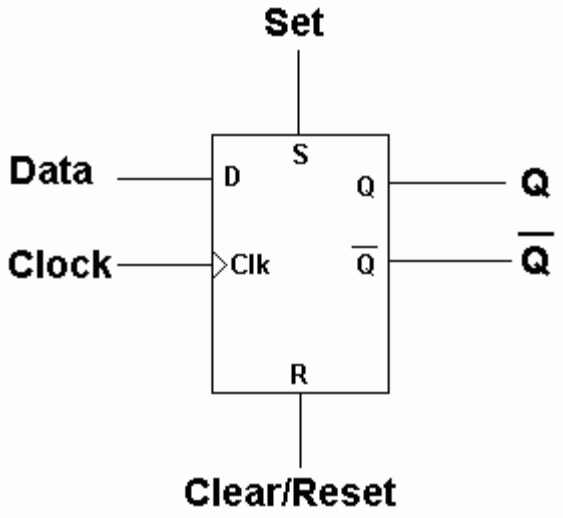
In this fashion, it is possible to *strobe* or *clock* the flip-flop in order to store information (set it or reset it) at any time, and then hold the stored information for any desired period of time. This flip-flop is called a *clocked RS flip-flop*. The proper symbol and truth table are given in Fig. 8–10*b*. Notice that there are now three inputs—R, S, and the ENABLE or CLOCK input, labeled CLK. Notice also that the truth-table output is not simply Q, but Q_{n+1}. This is because we must consider two different instants in time: the time before the ENABLE goes low Q_n and the time just after ENABLE goes low Q_{n+1}.

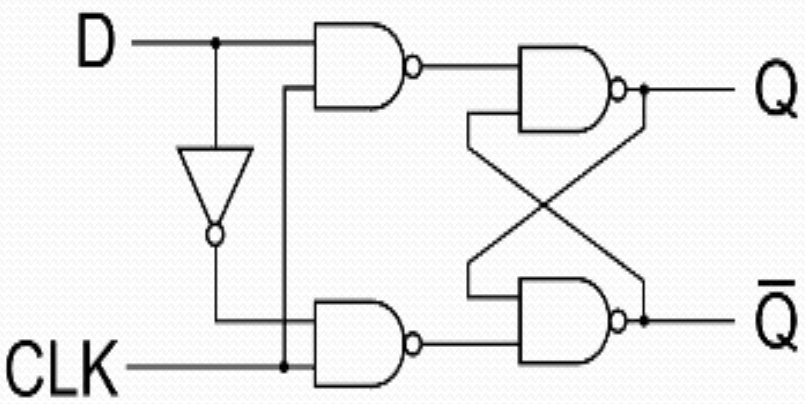
D- Flip Flop:

Drawbacks of RS FF:

- The RS FF has two inputs, the generation of two signals to drive a FF is a disadvantage.
- The forbidden condition of both R and S HIGH may occur inadvertendly

This has led to the D-FF :





The Truth Table & Timing Diagram for D-FF

Clock	D	Q_{next}
Rising edge	0	0
Rising edge	1	1
Non-Rising	X	Q